REMARKS

This is an amendment under 37 CFR §1.116. The purpose of this amendment is to correct an inadvertent error in claim 9, and to respond to the reference citations and arguments made by the Examiner in the last office action. Since this response is being filed within two months of the mailing date of the final rejection, the courtesy of an advisory action is respectfully requested.

Claims 1-9 are in this application. Claims 3-8 have been allowed. Claim 9 was amended to correct an inadvertent error in the claim dependency. (The limitations of claim 9 are recited in claim 3.)

The Examiner rejected claims 1 and 2 under 35 U.S.C. §103(a) as being unpatentable over Klein (U.S. Patent No. 4,205,330) in view of Takagi (U.S. Patent No. 4,003,071). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 1 recites, in part:

> "a layer of second gate oxide formed over the second channel, the layer of second gate oxide having a thickness, . . ., the thickness of the layer of first gate oxide being substantially less than the thickness of the layer of second gate oxide."

In rejecting the claims, the Examiner pointed to the Klein reference as teaching an enhancement-mode transistor and a depletion-mode transistor, where the depletion-mode transistor has a shorter channel length than the enhancement-mode transistor. (See, for example, FIG. 3g of Klein.) The Examiner also noted that Klein does not show enhancement-mode and depletion-mode transistors that have gate oxide layers with substantially different thicknesses, but argued that it would be obvious to use a thicker layer of gate oxide with the enhancement-mode transistor of Klein in view of Takagi.

With respect to Takagi, the Examiner pointed to FIG. 6A as showing a gate insulating film 65 of an enhancement-mode transistor 62 that is thicker than a gate insulating film 66 of a depletion-mode transistor 63. In addition, the Examiner, citing column 8, lines 17-34 of Takagi, noted that gate insulating film 66 of depletion-mode transistor 63 permits the formation of an impurity diffused layer (the depletion channel), whereas gate insulating film 65 of enhancement-mode transistor 62 prevents this from happening.

The Examiner then argued that one skilled in the art would be motivated to form the gate oxide regions of Klein with substantially different thicknesses as shown in Takagi to form only the layers that are necessary for enhancement and depletion mode transistors, and to save manufacturing steps. One skilled in the art, however, would not be motivated to combine the two references as suggested by the Examiner.

FIGS. 3a-3h of Klein show a series of process steps for forming a depletion-mode transistor and an enhancement-mode transistor. FIGS. 3b-3c of Klein show the implantation of boron into a p-type substrate 20, and the subsequent diffusion of the boron to form a p-region 25 with a specific resistivity. (See column 3, lines 66-68 of Klein.) Klein also teaches that a controlled resistivity is required to make enhancement-mode transistors with a desired threshold voltage. (See column 2, lines 13-15 of Klein.)

FIGS. 3d and 3e of Klein show the implantation of phosphorous into a p-type substrate 20 and p-region 25. The phosphorous implant forms a channel region 30a of the depletion-mode transistor. In addition, the implant also sets the threshold voltage of the to-be-formed enhancement-mode transistor to the desired value. (See column 4, lines 19-21 of Klein.) Further, FIGS. 3f and 3g show the implantation of phosphorous to form n+ regions 35-38 that function as the source and drain regions of the depletion-mode transistor and the enhancement-mode transistor. (See column 5, lines 10-13 of Klein.)

It is unclear how the Examiner proposes to combine Takagi into Klein to form only the necessary layers and reduce manufacturing steps. Assume, for example, that the thickness of the oxide layer under gate 32 and the implant energy were increased so that depletion channel 30a shown in FIG. 3f of Klein could be formed during the same implant step that forms the source/drain regions in FIG. 3f/g.

This assumption, however, does not allow any of the manufacturing steps shown in Klein to be eliminated. This is because the implant shown in FIG. 3d of Klein, where Klein originally formed depletion channel 30a, must still be performed to set the threshold voltage of the enhancement-mode transistor. Thus, combining the Takagi reference into the Klein reference does not eliminate any manufacturing steps.

Further, one skilled in the art would not be motivated to form the depletion channel 30a of Klein as part of a high energy implant step. This is because a high energy implant, such as the implant step shown in Takagi, would have to be driven through gate oxide layer 29a to form the depletion channel 30a, potentially damaging gate oxide layer 29a. The implant shown in FIG. 3d of Klein, on the other hand, can not damage gate oxide layer 29a because the implant occurs before gate oxide layer 29a is formed.

Thus, one skilled in the art would not be motivated to incorporate the Takagi reference into the Klein reference to save manufacturing steps because no manufacturing steps are saved. As a result, claim 1 is patentable over Klein in view of Takagi. In addition, since claims 2 and 9 depend from claim 1, claims 2 and 9 are patentable over Klein in view of Takagi for the same reasons as claim 1.

Thus, for the foregoing reasons, it is submitted that the application is in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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